What is claimed is:

1. A solid-state image sensing device having at least one pixel, said pixel comprising:

a photoelectric conversion section for outputting an electric signal according to a quantity of incident light; and

a sample hold circuit for sampling and holding the electric signal from the photoelectric conversion section and outputting the sampled and held electric signal as an image signal,

wherein a reset voltage for resetting the sample hold circuit obtains at least two different values.

2. A solid-state image sensing device claimed in claim 1, wherein the electric signal is a voltage signal, and when the electric signal is sampled and held by the sample hold circuit, the reset voltage is set to a value which is different from the value of the voltage for resetting the sample hold circuit.

3. A solid-state image sensing device claimed in claim 1, wherein the at least one pixel has a switch for electrically connecting and disconnecting the photoelectric conversion section and the sample hold circuit.

4. A solid-state image sensing device claimed in claim 3, wherein a plurality of sets of the pixels are provided, and wherein the photoelectric conversion sections and the switches operate at a same timing with respect to all the pixels, and the electric signals obtained by the imaging at the same timing are sampled and held by the sample hold circuits on the pixels, respectively.

5. A solid-state image sensing device claimed in claim 4, wherein, after the sample hold circuits are rest, the switches are turned on, so that the electric signals from the photoelectric conversion sections are given to the sample hold circuits.

6. A solid-state image sensing device claimed in claim 1, wherein the reset voltage is set to a first voltage during pixel reset time where the pixels are reset, and the reset voltage is set to a second voltage during time other than the pixel reset time, and wherein the pixel reset time includes starting time of the reset of the sample hold circuits through time before output of the image signals from the sample hold circuits.

7. A solid-state image sensing device claimed in claim 1, wherein the reset voltage is set to a first voltage during the sample hold circuit reset time where the sample hold circuits are reset, and the reset voltage is set to a second voltage during time other than the sample hold circuit reset time.

8. A solid-state image sensing device claimed in claim 1, wherein the photoelectric conversion section includes:

a photoelectric conversion circuit for generating an electric charge according to a quantity of incident light; and

an integrating circuit for outputting a voltage obtained by accumulating the electric charge from the photoelectric conversion circuit as the electric signal.

9. A solid-state image sensing device claimed in claim 8, wherein the integrating circuit comprises a capacitor for accumulating the electric charges output from the photoelectric conversion circuit.

10. A solid-state image sensing device claimed in claim 8, wherein the reset

voltage to be applied to the sample hold circuit is also applied to the integrating circuit.

11. A solid-state image sensing device claimed in claim 8, wherein a DC reset voltage with a constant value which is different from the reset voltage to be given to the sample hold circuit is applied to the integrating circuit.

12. A solid-state image sensing device claimed in claim 8, wherein the sample hold circuit comprises a capacitor for sampling and holding the electric signal.

13. A solid-state image sensing device claimed in claim 12, wherein the sample hold circuit further includes a transistor having a first electrode, a second electrode to which the capacitor is connected, and a control electrode into which a voltage from the integrating circuit is inputted, and wherein a voltage which appears at a connecting node between the second electrode of the transistor and the capacitor serves as the image signal.

14. A solid-state image sensing device claimed in claim 1, wherein the sample hold circuit includes an output switch for electrically connecting and disconnecting an output signal line and the capacitor, the output line being for outputting the electric signal as the image signal.

15. A solid-state image sensing device claimed in claim 14, the photoelectric conversion section outputs an electric signal which is linearly converted with respect to the quantity of the incident light.

16. A solid-state image sensing device claimed in claim 14, the photoelectric conversion section outputs an electric signal which is converted logarithmically with respect to the quantity of the incident light.

17. A solid-state image sensing device claimed in claim 8,

wherein the at least one pixel has a switch for electrically connecting and disconnecting the photoelectric conversion section and the sample hold circuit.

wherein the integrating circuit comprises a first capacitor, while the sample hold circuit comprises a second capacitor and a transistor, and

wherein the solid-state image sensing device further comprises:

a first reset switch, connected with one end of the first capacitor for resetting the first capacitor;

a second reset switch connected with a control electrode of the transistor; and

a third reset switch, connected with one end of the second capacitor, for resetting the second capacitor.

18. A solid-state image sensing device claimed in claim 17, wherein the switch and the second reset switch are turned on, so that the first capacitor and the control electrode of the transistor may be reset simultaneously.

19. A solid-state image sensing device claimed in claim 1, wherein the at least one pixel comprises an output circuit for amplifying the voltage output from the sample hold circuit and outputting the image signal.

20. A solid-state image sensing device claimed in claim 1, wherein the at least one pixel outputs the electric signal which changes in a logarithmic manner with respect to the quantity of the incident light.

21. A solid-state image sensing device claimed in claim 1, wherein the photoelectric conversion circuit is switched between a linear transforming operation for outputting the electric signal which changes linearly with respect to the quantity of the

incident light and a logarithmic transforming operation for outputting the electric signal which changes in the logarithmic manner with respect to the quantity of the incident light.

22. A solid-state image sensing device claimed in claim 1, wherein the at least one pixel further comprising an FET switch through which the reset voltage is applied to the sample hold circuit.

23. A solid-state image sensing device claimed in claim 22, wherein the reset voltage is applied to the sample hold circuit while the FET switch is turned on.

24. A solid-state image sensing device claimed in claim 23, wherein the at least two different values of the reset voltage include a first value and a second value.

25. A solid-state image sensing device claimed in claim 24, wherein the first value is set so as to be suitable for resetting the sample hold circuit, while the second value is set so as to suppress a leakage of electric charge from the sample hold circuit through the FET switch.

26. A solid-state image sensing device claimed in claim 25, wherein a voltage difference between a source of the FET switch and a drain of the FET switch when the reset voltage having the second value is applied is smaller than that reset voltage having the first value is applied.

27. A solid-state image sensing device claimed in claim 26, wherein the FET switch comprises a P-channel MOS transistor, and wherein the second value is lower than the first value.

28. A solid-state image sensing device claimed in claim 26, wherein the FET switch comprises an N-channel MOS transistor, and wherein the second value is higher than the first value.

29. A solid-state image sensing device claimed in claim 24, wherein the second value is set so as to suppress a leakage of electric charge from the sample hold circuit.